Analysis of Clock Signals Imperfections and Their Impact on an N-path Frequency Down-converter

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***Abstract* — This paper describes new impact analyses carried out on the imperfections of clock signals in the innovative but not well-known N-path Frequency Down-converter. Using an evolution of a previously developed analytical model, these analyses give more insight on the performance of the N-path Frequency Downconverter and allow more precise trouble-shooting of an IC realized on this principle. They are compared with measurements.**

***Keywords* — Frequency conversion, model, N-path filter, passive mixer, down-converter, non-idealities analysis.**

I. Introduction

Studied from the middle of the 20th century, N-path circuits have recently been in the spotlight because of their ability to solve flexibility and adaptability upcoming challenges, with intrinsic programmable parameters (input and output center frequencies, bandwidth, delay). Many applications are proposed for topical issues at 5G frequencies [1] or for Internet of Things (IoT) systems [2].

These circuits, although having potential in Software Defined Radio (SDR) systems, are generally complex to design and to analyze. Recent works aim at giving more insight on the behavior of N-path circuits [3], and on the impact of non-idealities, such as unmatched impedances [4], or switch capacitance [5].

Unlike the other N-path principles, the N-path Frequency Downconverter is not on the scope of many analyses nor design works, although it has the particular feature of converting an input frequency band into an output frequency band, without modifying bandwidth. Fig. 1 gives an example of an ideal 4-path Frequency Down-converter schematic with ideal clock signals. The precise behavior is described in [3].

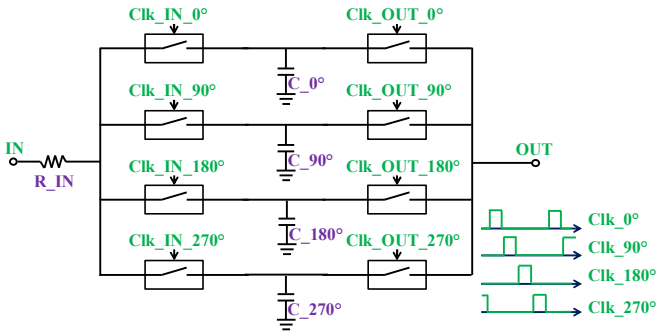

Fig. 1. (Fig. 1. From [3]) The ideal 4-path Frequency Down-converter, with corresponding clock signals

The goal of this paper is to analyze the effect of clock signals imperfections in this circuit. For this purpose, the common aspects and parameters of the presented analyses will be synthesized in part II, followed by the rise and fall times impact analysis in part III, the dissymmetries impact analysis in part IV, and the retro-simulation of a measured Integrated Circuit (IC) in part V.

II. Overall Analyses Presentation and Common Important Parameters

The present analyses compare a mathematic model, and an electrical simulation. The following sections refer to these two by "model" and "simulation" respectively.

The reference circuit on which the comparisons are made is the 4-path of Fig. 1.

The mathematic model, of which evolution results are shown in this paper, corresponds to the one presented in [3], with a modification of the Fourier coefficients to describe the N-path Frequency Down-converter in case of trapezoidal clock signals.

For the electrical simulation made with Cadence® Spectre® PSS analysis, a configurable N-path Frequency Down-converter has been defined. It incorporates adjustable frequencies, passive component values, input power, switches and clock signals parameters.

Both model and simulation share the same main parameters, which were also used in [3], as follows:

- input clock frequency : 1.5 GHz
- output clock frequency : 0.4 GHz
- input signal frequency (for output spectra) : 1.45 GHz
- paths capacitors : 3,5 pF

The off-state resistances for the switches are set as infinite, in order to prevent inter-paths effects. The simulation uses a common resistor of 50 Ω, and an on-state resistance of 40 Ω for the input switches, but these two values are respectively 0 Ω and 90 Ω for the model, because it cannot take into account a non-zero common resistor causing inter-paths coupling effects.

Unless otherwise specified, input power is fixed at 0 dBm.

At this stage, only the input clock signals modifications are analyzed. The global clock signals modifications analysis, which comes with intercorrelated effects, will be performed in future works. Thus, the output clock signals remain the same as those of the ideal case.

III. Impact Analysis of Rise and Fall Times of Clock Signals

The goal of this first analysis is to determine whether or not the rise and fall times of the clock signals impact the overall response of the N-path Frequency Down-converter. Both the model and simulation have been exploited for this purpose.

A. Analysis Conditions

Four cases, shown in Fig. 2, are compared and analyzed: no rise/fall times, non-zero equal rise/fall times, only rise time, and only fall time. It is to be noted that, for every one of this four cases, the half-height time remains the same.

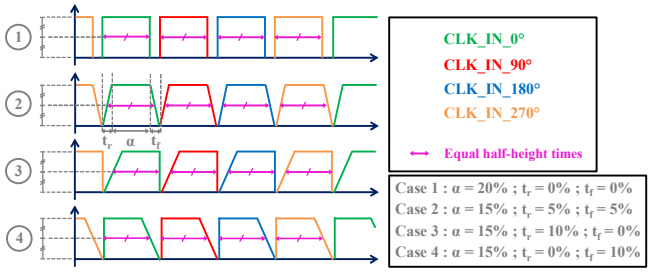

Fig. 2. The different analyzed cases with rise time t_r, fall time t_f and duty cycle α expressed as percentages of period

B. Impact on the Main Conversion Gain

Fig. 3. gathers the main conversion gains obtained with both the mathematic model and the electrical simulation, for the four cases depicted in Fig. 2.

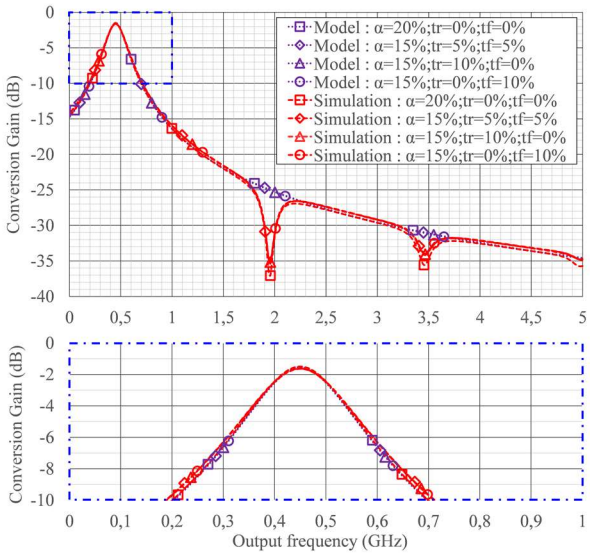

Fig. 3. Mathematical model and electrical simulation results for main conversion gain (i.e. frequency translation corresponding to frequency difference between input and output clocks) in the different cases of rise time, fall time, and duty cycle.
Top: large frequency span; Bottom: zoom around useful frequency band

The observed discrepancy in large bandwidth is due to lack of high enough complexity order of the model ([3]) but is not relevant for our analysis here. The model and simulation curves match well in the passband, with a maximum difference of 0.5 dB, validating the capability of the model to describe rise and fall times for the input clock signals.

Moreover, there are no significant differences in the main conversion gain between the four cases. The maximum deviation is about 2 dB around the minimum of the simulation curve, at –35 dB.

C. Impact on the Output Spectrum

To complete this analysis, output spectra obtained for the four cases are also compared in Fig. 4.

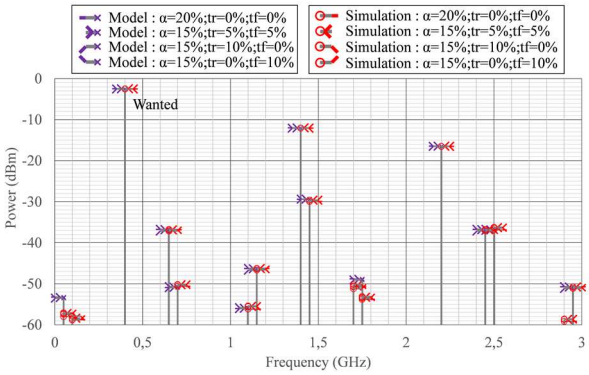

Fig. 4. Mathematical model and electrical simulation results for output spectrums in the different cases of rise time, fall time and duty cycle

The same conclusions can be drawn for the output spectra. The electrical simulation validates the analytical model results for the different four cases, and the tones values are very close between them, especially for the main in-band spectral lines.

D. Analysis Outcomes

These results lead to the conclusion that for trapezoidal signals, rise and fall times and duty cycle have no impact as long as the half-height duration stays constant. The expressions of the Fourier coefficients of the clock signals, which define the N-path Frequency Down-converter response (i.e. (8) of [3]), are mainly related to this last predominant parameter. The variations of the rise and fall times or the duty cycle for constant half-height duration will only create a detectable difference for high indices coefficients, which causes negligible deviations of the Harmonic Transfer Functions (HTF), as predicted by the model, leading to the observed results.

From the design point of view, we can conclude that the sharpness of the clock pulse waves is not as important as for other classical circuits, leading to relaxation of maximum frequency constraints for technological node and clock generation. It is also to be noted that the dissymmetry of the rise and fall times, which is often observed in MOS logic circuits, is not an important issue to deal with.

IV. Impact Analysis of Dissymmetries of Clock Signals

The second analysis aims to determine the impact of the so called dissymmetries between clock signals. We talk about dissymmetries in an N-path Frequency Down-converter when the different paths clock signals parameters differ between them in the same group (input or output clocks). For phases, which are equally distributed over the period in the ideal case, the

clock signals are dissymmetric when a deviation exists from this distribution, e.g. quadrature phases for a 4-path.

A. Analysis Conditions

This analysis is carried on with no rise/fall times (as this has been shown non relevant) and the different duty cycles set to have one and only one clock signal at on-state at every time.

The two main dissymmetries are presented in Fig. 5.

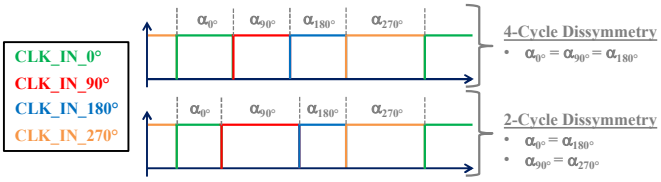

Fig. 5. Representation of the clock signals for the two types of analyzed dissymmetries

4-Cycle and 2-Cycle dissymmetries mean respectively that one out of four and one out of two signals exhibit the same parameters, or phase deviation from ideal case.

In the 4-Cycle case, the first free clock signals exhibit an identical duty cycle, while fourth completes clock period. For 2-Cycle, the first and third signal have the same duty cycle, and second and fourth complete a half-period.

B. Impact on the Output Spectrum

The results of the simulation are regrouped in Fig. 6. The dissymmetries are expressed as a percentage of the period and they refer to the deviation of the fourth clock signal duty cycle from the ideal value of 25%. The other three clock signals duty cycles are adapted with respect to the rules presented in Fig. 5.

For main tones, the powers remain globally unchanged, with a maximum difference of 1 dB, whereas many parasitic tones appear with dissymmetries.

4-Cycle dissymmetry generates spurious frequencies around each multiple of the clock frequency, except the fourth multiple and its harmonics, the most powerful being around even harmonics of the clock signal. 2-Cycle dissymmetry generates spurious frequencies only around odd harmonics. These 2-Cycle tones correspond to the image frequencies of the ideal case spectral lines, i.e. mirrored frequencies of this spectral lines around nearest clock harmonics.

For both dissymmetries, the power of the parasitic tones increases with the importance of the dissymmetries.

C. Analysis Outcomes

In the ideal case of the N-path Frequency Down-converter, the Harmonic Transfer Functions described in part III.*A* of [3] are null when the sum of input and output harmonic numbers of the HTFs are not equal to a multiple of the number of paths. When dissymmetries occur, the phase and amplitude of the outputs of the paths do not match perfectly to cancel the HTFs which don't satisfy the harmonic numbers sum condition. Fig. 7. synthesizes graphically the phenomenon, with the representation used in [1] to analyze the harmonic transfers.

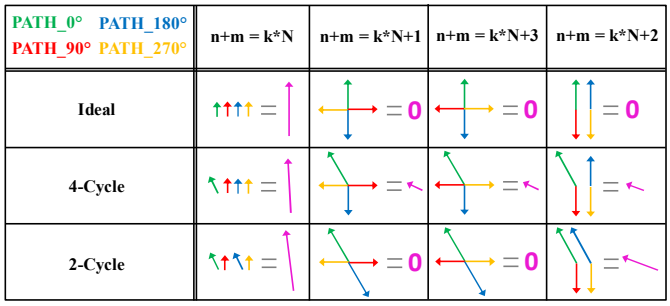

Fig. 7. Synthesis of the outputs of the different paths, depending on HTFs input and output harmonic numbers n and m, for ideal and dissymmetric cases. k is a negative or positive integer. Vectors are shown for qualitative purposes only.

Consequently, this leads to new spurious tones corresponding to these HTFs. In fact, all the combinations of input and output harmonics can occur, as it is the case for a 1-path circuit.

The 4-Cycle dissymmetry exhibits this behavior, because the fourth path input clock signal evolves independently from the others signals, whereas, for 2-Cycle, as the clock signals still correspond by pairs, the circuit can be assimilated to the sum of two 2-path circuits, in which HTFs remain null when the sum of the harmonic numbers are not equal to multiples of the number of paths, becoming 2 in this case.

No significant spurious frequencies exist around multiples of four times the output clock frequency because the corresponding Fourier coefficients of clock signals (multiple of four indices) are very close to, if not equal to, zero.

In contrast to rise and fall times, particular care must be taken with dissymmetries for the design of N-path Frequency Down-converter, to avoid high power spurious frequencies.

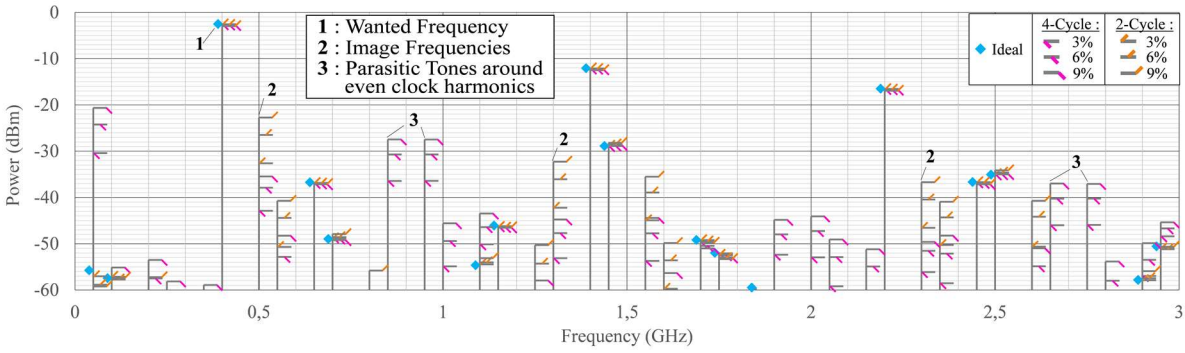

Fig. 6. Electrical simulations results for the output spectra in the different cases of clock signals dissymmetries

V. Application to Trouble-Shooting of a Measured 4-path Frequency Down-converter

Measurements have been carried on a 4-path Frequency Converter IC presented in part IV of [3]. These results show several deviations from the ideal case, that this part aims to explain for some of them.

A. Extraction of IC Clock Signals Main Characteristics

Typical simulated clock signals of the 4-path Frequency Converter IC are presented in Fig. 8.

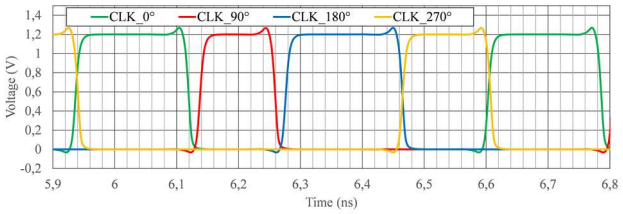

Fig. 8. Typical simulated 4-path Frequency Converter IC clock signals for a clock frequency of 1,5 GHz

These waveforms are valid for both input and output clocks, as the same clock generation circuit is used for both groups.

Using the outcomes of the rise and fall times impact analysis, and neglecting overlap effects, half-height durations are directly used as an equivalent of duty cycles to compare the four clock signals.

Then, considering that second and fourth signals have the same duty cycle, the 4-Cycle and 2-Cycle dissymmetries are about 3% and –5% respectively.

B. IC Output Spectrum Explanations with the Two Impact Analyses Outcomes

Measurements of the 4-path Frequency Converter were carried on with an input power of –26 dBm, and so are the simulations used for comparison.

The path capacitors value is 3.5 pF, the common resistor corresponds to the 50 Ω series resistor of the input generator, and the switches are designed to have 40 Ω on-state resistance.

The other main parameters are that of part II description.

Fig. 9. synthesizes the different types of tones that appear on the IC output spectrum, with ideal simulation results as a reference, also compared with retro-simulation with previously determined dissymmetries values.

The parasitic tones that correspond to the two types of dissymmetry are clearly visible on the figure:

- image frequencies are associated to 2-Cycle
- tones around even clock harmonics in addition to image frequencies are associated to 4-Cycle

However, dissymmetries do not describe all parasitic tones, and amplitude differences still remain for predicted tones. Clock leakage at the output buffer combined with decoupling circuits imperfections may be another main cause of this spurious frequencies, especially the multiples of the output frequency, as shown by a sensitivity analysis under way and not presented here.

In the end, retro-simulation spectral lines frequencies match well with corresponding measurements tones, identifying dissymmetries as an important cause of these.

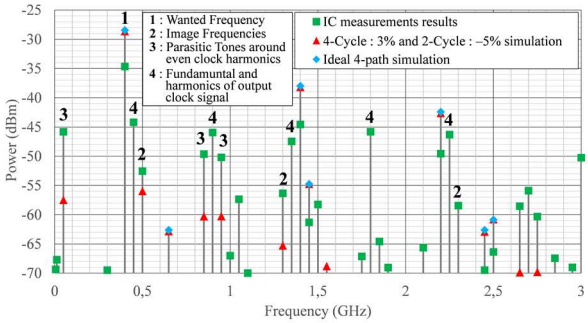

Fig. 9. Measured 4-path Frequency Converter IC, retro-simulated with IC clocks observed dissymmetries values configurable 4-path, and simulated ideal 4-path output spectrums for an input power of -26 dBm.

VI. Conclusion

Impact analyses have been carried on for clock signals imperfections of a 4-path Frequency Down-converter, with the use of a simulation-validated evolution of a previously developed analytical model. These allow better understanding and trouble-shooting of rise time, fall time, and clock dissymmetries issues in N-path Frequency Down-converters. It represents an important step for the optimization of future designs of these circuits. In the next design, clock signals generation circuits will be optimized for low dissymmetry.

Acknowledgment

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