PLL Unwrapping Structures using Polynomial Prediction Algorithm for Noisy Carrier Phase Tracking

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BIOGRAPHIES

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Lionel Ries is head of the Signal and RadioNavigation department of the CNES Radiofrequency sub-directorate since august 2009. He was a navigation engineer in the Transmission Techniques and Signal Processing department, at CNES since June 2000. He is one of the CBOC inventors. He graduated from the Ecole Polytechnique de Bruxelles, at Brussels Free University (Belgium) and received a M.S. degree from ISAE in Toulouse (France).

Paul Thevenon is a GNSS engineer in the GNSS signal processing team of CNES (Centre National d'Etudes Spatiales), the French space research center. He graduated as electronic engineer from Ecole Centrale de Lille and obtained a research master at ISAE (Institut Supérieur de l'Aéronautique et de l'Espace) in space telecommunications. Thevenon later obtained a Ph.D. degree in the signal processing laboratory of ENAC (Ecole Nationale de l'Aviation Civile) in Toulouse, France, studying the feasibility of self-positioning a receiver using mobile TV signals. His current activity is GNSS signal measurement and processing, with an emphasis on urban environment.

ABSTRACT

Since the rise of technologies using GNSS positioning systems, development of carrier phase tracking receiver for precise point positioning in hostile environments is becoming one of the most important challenges for future satellite navigation applications. Because phase locked loops (PLL) that track carrier phase suffer from cycle slips phenomenon, noise robustness of the formers has to be reinforced if one wants to use precise positioning techniques in the widest range of challenging environments.

The purpose of this article is to propose a new PLL design using a phase unwrapping algorithm that effectively corrects cycle slips due to phase noise in low CN0. Unlike phase unwrapping algorithms using a threshold approach for cycle slips detection, the algorithm implemented in our PLL structure is based on a system of prediction and pre-compensation of the phase dynamic stress. In order to reduce the cycle slips and enforce noise robustness of phase tracking, this algorithm is adapted to tracking loops with the aim to propose two innovative PLL structures. A comparative study is performed to show the effectiveness of the two proposed structures in case of noisy environment.

INTRODUCTION

Over the last years, precise point positioning (PPP) techniques have considerably progressed in terms of precision. Current PPP methods use accurate orbital data, accurate satellite clock data and carrier phase observations collected by GNSS receiver to estimate user pseudo-ranges [1,2]. Phase tracking is realized via phase locked loops (PLL) which have to provide accurate estimation of carrier phase. Although user positioning is more precise with carrier phase data than with code phase data [3], phase estimation suffers from a lack of robustness in case of low carrier-to-noise-density-ratio (CN0), thereof preventing using such techniques in a large number of hostile environments such as urban canyons. It also prevents this new appealing technique from being used in one of the main GNSS outlet, the mass market.

Besides, the new generation satellites navigation systems offer now pilot tone signals allowing envisaging new tracking techniques to reach higher performances, in particular for urban users. But even with this new signals the critical aspect remains the carrier phase tracking loop when it question of high accuracy in bad reception conditions.

One of the most important problems with noisy carrier phase tracking is cycle slips. Cycle slips are a distinctive characteristic of PLLs which directly results from the periodic nature of phase discriminators used in tracking loops [4]. These biases (the cycle slips), that can appear during the phase estimation and make the tracking fail, can be caused by either a high dynamic stress and/or a high noise level, including the consequences of signal fading due to multipath.

Several techniques aimed at detecting and correcting cycle slips have already been developed and adapted to PLL [5,6]. Basically, they rely on a threshold approach that try to correct cycle slips by comparing the discriminator output with the previous output to determine, by thresholding, if a cycle slip has occurred or not. However, due to the nonlinear nature introduced by thresholding, these structures are not robust to noise and do not provide an adequate phase tracking for precise positioning in low CN0 environments. It is possible to add a filtering step for this unwrapping structure (i.e., the filter involved is the inverse system of the unwrapping structure under linear approximation) that improves the noise robustness [6], but this step is not efficient enough in challenging environments.

What is proposed in this paper is two new PLL structures including a phase unwrapping system that offers better robustness to noise. More precisely, the phase unwrapping algorithm used for our PLL structures is based on a phase polynomial prediction and pre-compensation to anticipate cycle slips [7]. The first proposed PLL structure consists in analyzing phase discriminator outputs, thanks to the weighted recursive least squares algorithm (WRLS) [8], with the aim to predict the next phase error estimation output and pre-compensate it into the local replica in order to reduce the phase dynamic stress.
The second proposed PLL structure takes advantage of the low-pass nature of loop filter [9-11]. Indeed, in this PLL structure, the system of pre-compensation is unchanged but prediction is now performed by analyzing loop filters outputs. However, since filter outputs represent information about the instantaneous carrier frequency, an additional step is necessary to convert frequency prediction into discriminator output prediction. A conversion step is thus proposed to estimate the next discriminator output thanks to the loop filter analysis.
This article is divided in four parts. The first part introduces the general PLL structure and notations as well as the incoming signal model used in this paper. The second and third parts respectively deal with the first and the second proposed PLL structures and detail the two proposed algorithms. The last part is a comparative study which highlights the efficiency of the two proposed structures in term of noise robustness.

SIGNAL MODEL AND GENERAL PLL STRUCTURE

Before studying the proposed PLL structures, let us introduce some notations and definitions.

Signal model

The incoming signal *s[n]* is supposed to be a complex exponential signal. As code delay and data navigation synchronization are supposed to be established, the generation of the signal does not include neither Gold codes nor navigation data bits. The latter assumption is also supported by the future possibility to work on data pilot signal (GALILEO) [12]. We can therefore model the incoming signal as

$$s[n] = \sqrt{P}.\exp(2i\pi.\phi[n]) + b[n] \tag{1}$$

with P the received signal power, $\phi[n]$ the carrier phase to be tracked and $b[n]$ the white Gaussian thermal noise

$$b[n] \propto \mathrm{N}(0,\sigma^2). \tag{2}$$

The thermal noise power σ^2 is given by

$$\sigma^2 = \frac{P}{CN0} \times Fe \tag{3}$$

with $CN0$ the carrier-to-noise-density-ratio and F_e the incoming signal sample rate.

General PLL structure

Basic PLL structure and notations are given in Fig. 1. According to this figure, we define *s[n]* as the incoming signal, $\delta\theta[n]$ the estimated phase error (phase discriminator output) that is estimated from the correlation output $f(\delta\theta[n])$, $\dot{\theta}[n]$ the loop filter output, $\theta[n]$ the estimated Doppler phase of the incoming signal and $s_r[n]$ the local replica.

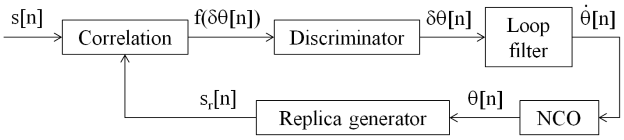

Fig. 1: Structure and notations of a standard PLL.

We suppose, in the following, to work either on an ATAN or an ATAN2 phase discriminator [14] and a second order PLL. Loop filter integrators and the NCO (Numerically-Controlled Oscillator) are modeled according to the rate-only feedback approach illustrated in Fig. 2, which means that if *x[n]* and *y[n]* denote respectively the input and the output of the integrator, one has

$$y[n] = y[n-1] + \frac{T}{2}(x[n-1] + x[n]) \tag{4}$$

with T the loop sample time (which corresponds to the correlation time). Numerical loop filter coefficients are chosen as a function of the loop bandwidth B_L as described in [13].

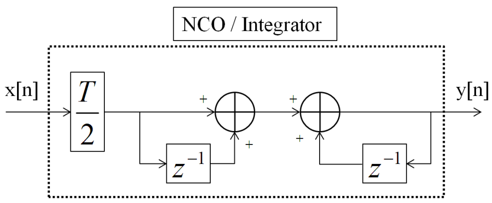

Fig. 2: NCO and Integrator rate-only feedback approach.

FIRST UNWRAPPING PLL STRUCTURE: ANALYSIS OF PHASE DISCRIMINATOR OUTPUTS

Overview of the PLL

If we want to enforce noise robustness of phase locked loops, we have to deal with the cycle slips phenomenon. To do so, we propose in this paper to incorporate into PLLs a phase unwrapping algorithm which offers better noise robustness than algorithms based on a threshold approach for cycle slip detection. This unwrapping algorithm relies on a polynomial phase model prediction which aims at anticipating cycle slips [7].

Since cycle slips occur during the phase estimation error step, the first adaptation of the unwrapping algorithm is to make it predict the next discriminator output. Indeed, if one can predict the forward phase estimation error $\delta\theta[n+1]$, a pre-compensation step can be realized to anticipate this evaluation at the next step of error estimation. By doing so, the phase dynamic stress estimated by the phase discriminator is reduced and occurrence of cycle slip is then lessened. Because these cycle slips are due to a critical combination of phase dynamics and noise, pre-compensating the dynamic stress allows the phase discriminator to sustain a higher phase noise power. In light of this remark, the new PLL structure is then expected to be more robust to phase noise.

General scheme of the new PLL structure is given in Fig. 3. More precisely, the new structure is operating as follows: at each step of loop iteration, a prediction of the next phase discriminator output is performed thanks to the past outputs. Algorithm used for this estimation is the weighted recursive least square algorithm (WRLS) [8]. Once the prediction calculated, we can use it to pre-compensate it both for local replica generation and at the discriminator stage. This operation reduces the tracking phase dynamics. Notice that a gain K is added before pre-compensating to reduce prediction error effect. Obviously, this gain will be chosen such as $K \leq 1$.

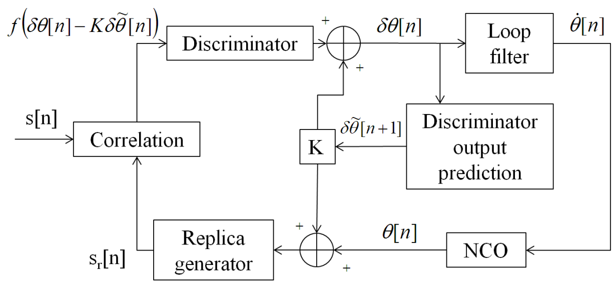

Fig. 3: PLL unwrapping structure analyzing phase discriminator outputs.

So far, the new PLL structure has been defined; calculation steps of phase discriminator output prediction and pre-compensation are now detailed.

Discriminator output polynomial model

In order to predict the next phase discriminator output thanks to the WRLS algorithm, an analysis model of the former has to be established. The model chosen for the prediction step is an M degree polynomial approximation (which does not consider cycle slips phenomenon and assumes that the discriminator output is continuous), i.e.,

$$\delta\tilde{\theta}[n] = \sum_{k=0}^{M} a_k n^k + \varepsilon[n] \tag{5}$$

where $\varepsilon[n]$ is the perturbation due to phase noise. Parameters $\{a_0 \; \dots \; a_M\}$ are the polynomial phase coefficients that define our model. In this paper, the polynomial degree M will be constantly fixed to 1, i.e., we will suppose that the phase discriminator output can be approximated by a straight line. In practice, it is obvious that the discriminator output does not look like a line but, if we chose an sufficiently limited weight factor in the recursive least squares algorithm, this linear assumption is reasonable.

The polynomial model defined by expression (5) will allow us, by estimating the parameters $\{a_0 \ldots a_M\}$, to predict and pre-compensate the phase discriminator outputs thanks to the algorithm described next.

Algorithm of prediction and pre-compensation

The new PLL structure shown in Fig. 3 is based on an iterative unwrapping algorithm [7] which predicts and pre-compensates the phase discriminator output. Calculation steps of this algorithm are detailed further.

1-Initialization

To initialize the iterative algorithm of prediction/pre-compensation, we have to compute a first estimate of the polynomial parameters $\{a_0 \ldots a_M\}$. This initialization will be performed by analyzing the first phase discriminator outputs with the weighted least squares algorithm.

More precisely, let us assume to know the N first discriminator outputs $\boldsymbol{\Delta\theta}(N)= [\delta\theta[0],\delta\theta[1] \ldots\delta\theta[N\text{-}1]]^T$. According to the polynomial analysis model of the discriminator output (5), we can write the linear matrix equation,

$$\boldsymbol{\Delta\theta}(N) = \mathbf{G}(N)\mathbf{a} + \boldsymbol{\varepsilon} \tag{6}$$

where $\boldsymbol{\varepsilon}^T=[\varepsilon[0],\varepsilon[1],...\varepsilon[N-1]]$ is the phase noise vector, $\boldsymbol{a}^T= [a_0, a_1,\ldots,a_M]$ the polynomial parameter vector and the $N\times(M+1)$ auxiliary matrix $\boldsymbol{G}(N)$ is

$$\mathbf{G}(N) = \begin{bmatrix} 1 & 0 & 0^2 & \cdots & 0^M \\ 1 & 1 & 1^2 & \cdots & 1^M \\ 1 & 2 & 2^2 & \cdots & 2^M \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 1 & N-1 & (N-1)^2 & \cdots & (N-1)^M \end{bmatrix}. \tag{7}$$

The weighted least squares estimate for polynomial parameters is

$$\tilde{\mathbf{a}}(N) = \left(\mathbf{G}(N)^{\mathbf{T}}\mathbf{R}_N^{-1}\mathbf{G}(N)\right)^{-1}\mathbf{G}(N)^{\mathbf{T}}\mathbf{R}_N^{-1}\boldsymbol{\Delta\theta}(N) \tag{8}$$

where $\boldsymbol{R}_N$ is the weight matrix. In our study, we chose an exponential weight matrix $\boldsymbol{R}_N$=diag(1, $\lambda\ldots\lambda^{N\text{-}1}$) with λ the weight factor. It is chosen as $\lambda<1$ to respect the linear approximation (5).

2- Prediction of the next discriminator output

Using the polynomial parameters vector estimation $\tilde{\boldsymbol{a}}(n)$ (for $n\geq N$), we can estimate the next discriminator output. This prediction is given by

$$\delta\tilde{\theta}[n+1] = \mathbf{g}_{n+1}^T\tilde{\mathbf{a}}(n) \tag{9}$$

where $\mathbf{g}_{n+1}^T$ is the $(n+1)$th row of $\boldsymbol{G}(n+1)$, that is

$$\mathbf{g}_{n+1}^T = \begin{bmatrix}1 & n & n^2 & \cdots & n^M\end{bmatrix}. \tag{10}$$

3- Phase dynamics pre-compensation

Pre-compensation of the phase prediction computed at the previous stage is performed as follows

$$\delta\theta[n+1] = \angle\left(f\left(\delta\theta[n] - K\tilde{\theta}[n+1]\right)\right) + K.\delta\tilde{\theta}[n+1] \tag{11}$$

where $\angle(\cdot)$ is the studied discriminator angle function ATAN or ATAN2, i.e.,

$$\angle\left(f(\theta)\right) = \begin{vmatrix} \text{atan}\left(\Im(f(\theta)) \big/ \Re(f(\theta))\right) \\ \\ \text{atan2}\left(\Im(f(\theta)), \Re(f(\theta))\right) \end{vmatrix} \tag{12}$$

with the atan2 function defined as

$$\text{atan2}(x, y) = 2\text{atan}\left(\frac{y}{\sqrt{x^2 + y^2} + x}\right). \tag{13}$$

4- Polynomial coefficients updating

A new estimation of the coefficients parameters $\{a_0 \ldots a_M\}$ is performed by updating the last estimation thanks to the WRLS algorithm,

$$\mathbf{C}_{n+1} = \mathbf{P}_n\mathbf{g}_{n+1}^T\left(\lambda^{-n} + \mathbf{g}_{n+1}\mathbf{P}_n\mathbf{g}_{n+1}^T\right)^{-1} \tag{14}$$

$$\tilde{\mathbf{a}}(n+1) = \tilde{\mathbf{a}}(n) + \mathbf{C}_{n+1}\left(\delta\theta[n+1] - \mathbf{g}_{n+1}\tilde{\mathbf{a}}(n)\right) \tag{15}$$

$$\mathbf{P}_{n+1} = \mathbf{P}_n - \mathbf{C}_{n+1}\mathbf{g}_{n+1}\mathbf{P}_n \tag{16}$$

with $\mathbf{C}_n$ the gain vector and $\mathbf{P}_n$ the error estimation covariance matrix.

5- Iteration

Algorithm of prediction/pre-compensation is performed by iterating through steps 2-4 for each iteration step of the tracking loop.

Analysis of the PLL structure during the tracking

In order to verify the efficiency of the proposed PLL structure shown in Fig. 3, let us track a Doppler phase and observe the discriminator output. Fig. 4 shows us how the proposed PLL structure is operating to anticipate cycle slips. We can see on this figure both steps of prediction and pre-compensation of the phase unwrapping algorithm used for our PLL for a free noise phase tracking.

Doppler dynamics used for the experiment is fixed to 2Hz, i.e.,

$$\dot{\phi}(0) \Big/ 2\pi = 2Hz\,. \qquad (17)$$

The phase discriminator is chosen as an ATAN discriminator for this example (and because we assume to work on a C/A GPS signal) and all others parameters of the tracking loop are given in Fig. 4.

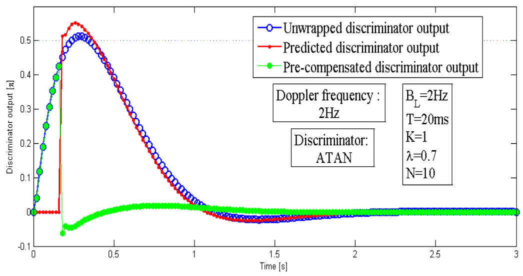

Fig. 4: Prediction and pre-compensation of discriminator output by analyzing discriminator output.

We can notice that during the tracking, the discriminator output exceeds the linearity range [-π/2, π/2] of the ATAN function. However, no cycle slips appears because discriminator output prediction is precise enough to anticipate it. Indeed, pre-compensation of the predicted output makes the phase discriminator estimate a lower phase dynamics and prevent the discriminator output from exceeding the linearity bound. Fig. 5 illustrates the estimation of the phase polynomial parameters $\{a_0, a_1\}$ during the track. We can see that, as expected, these two parameters tend to be null (for a second order PLL, there is no steady state error when tracking a frequency step).

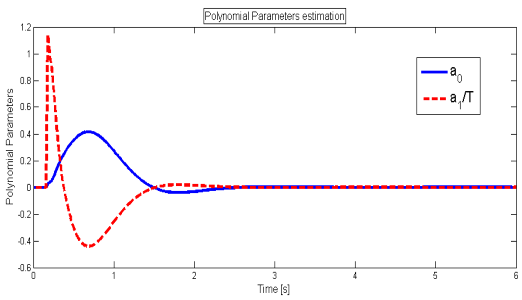

Fig. 5: Polynomial coefficients estimation for phase discriminator output analysis.

Fig. 6 shows the Doppler phase tracked by the proposed PLL structure and a conventional PLL. We can see that for the proposed PLL unwrapping structure, the cycle slips does not occur contrary to the basic PLL structure.

Efficiency of the proposed PLL structure for noisy phase tracking is studied in a later section.

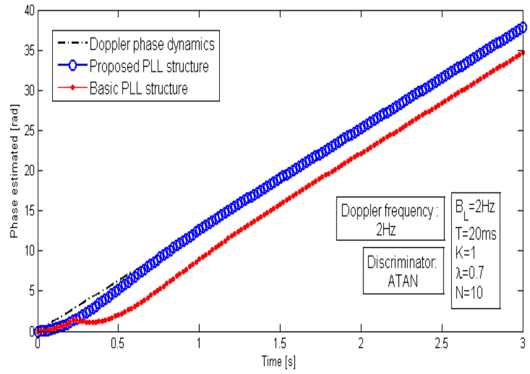

Fig. 6: Phase tracking for conventional and unwrapping PLL analyzing discriminator output.

SECOND UNWRAPPING PLL STRUCTURE: ANALYSIS OF LOOP FILTERS OUTPUTS

Overview of the PLL

The PLL structure described in the previous section analyses the phase discriminator output to predict the forward output and pre-compensate it. We now propose another new PLL structure that analyses the loop filter outputs to predict the next discriminator output. This new structure is illustrated in Fig. 7.

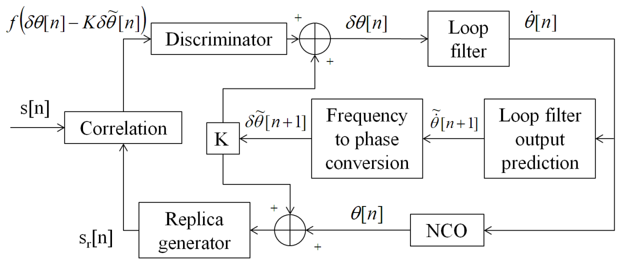

Fig. 7: PLL unwrapping structure analyzing loop filter outputs.

The aim of the structure in Fig. 7 is the same as the structure presented previously in Fig. 6: to predict and pre-compensate the phase dynamic stress in order to anticipate cycle slips. Pre-compensation stage is unchanged however the prediction is now calculated by analyzing the loop filter outputs. The main interest of this new configuration is to take advantage of the low-pass nature of the loop filter. Indeed, loop filter outputs are less noisy than the phase discriminator outputs, so predicting the former may be profitable regarding the noise robustness.

Algorithm of prediction and pre-compensation

As announced previously, the pre-compensation stage is the same as the one introduced in Fig. 3. The only difference is that prediction of the next discriminator output is realized by analyzing the loop filter outputs. To do so, we have to establish an analysis model of the loop filter output. As before, this model is chosen as an M order polynomial model:

$$\dot{\tilde{\theta}}[n] = \sum_{k=0}^{M} b_k n^k + \upsilon[n] \tag{18}$$

with $v[n]$ the noise component and $\{b_0 \ldots b_M\}$ the polynomial parameters we want to estimate. As for the former PLL structure, M will be constantly fixed to 1. The algorithm that recursively estimates the polynomial parameters is the same as described in the previous section.

Since loop filter outputs give information about the instantaneous carrier frequency, an additional step is necessary to convert frequency prediction into discriminator output prediction. This new calculation step is described hereafter.

Conversion of loop filter output prediction to phase discriminator output prediction

Working on loop filter output involves an additional calculation step that converts loop filter output prediction to phase discriminator output prediction. In order to perform this conversion, we have to express the discriminator output $\delta\Theta(n)$ as a function of the estimated polynomial coefficients $\{b_0,\ldots,b_k\}$. To do so, we use the phase discriminator output transfer function of the PLL described in Fig. 8,

$$\delta\theta(z) = \theta(z) - \theta_r(z) = \left(1 - H(z)\right)\theta(z) \tag{19}$$

with $\delta\Theta(z)$ the phase discriminator output, $\Theta(z)$ the phase dynamics we want to track, $\Theta_r(z)$ the phase estimation and $H(z)$ the linear closed loop transfer function of the PLL (i.e., the one that does not considers cycle slips phenomenon), i.e.,

$$H(z) = \frac{z^{-1}F(z)N(z)}{1 + z^{-1}F(z)N(z)} \tag{20}$$

with $F(z)$ and $N(z)$ the transfer functions of respectively the loop filter and the NCO [13].

Obviously, we do not know the expression of the tracked phase dynamics $\theta(z)$. To inverse the expression (19), we use an estimation $\tilde{\theta}(z)$ of the phase dynamics built with the estimated polynomial coefficients $\{b_0,\ldots,b_k\}$. These coefficients give us information about the frequency dynamics, i.e. (recall that M=1)

$$\dot{\tilde{\theta}}[n] = b_0 + b_1 n\,. \tag{21}$$

By integrating (21) and fixing the integration constant to 0, we obtain

$$\tilde{\theta}[n] = b_0 n + \frac{1}{2} b_1 n^2 \tag{22}$$

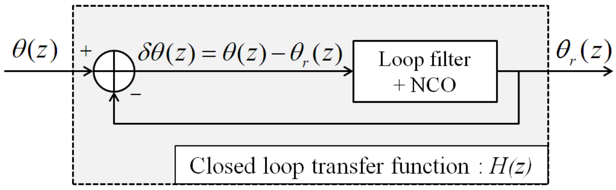

Fig. 8: Linear closed loop transfer function of the PLL.

The expression (22) does not include the correlation stage of the PLL. If we want to precisely estimate the discriminator output, we have to calculate the phase dynamics associated to the dynamics (22) affected by the correlation time T. By developing the expression of the correlation stage and neglecting some small correlation terms, we obtain the equivalent phase dynamics

$$\tilde{\theta}[n] = c_0 + c_1 n + c_2 n^2 \tag{23}$$

with

$$\begin{aligned} c_0 &= b_1 \frac{T^2}{6} - b_0 \frac{T}{2} \\ c_1 &= b_0 - b_1 \frac{T}{2} \\ c_2 &= \frac{1}{2} b_1 \end{aligned} \tag{24}$$

The phase dynamics expression (23) gives us [16]

$$\tilde{\theta}(z) = c_0 \frac{1}{1 - z^{-1}} + c_1 \frac{z^{-1}}{(1 - z^{-1})^2} + c_2 \frac{T^2 z^{-1}(1 + z^{-1})}{(1 - z^{-1})^3}\,. \tag{25}$$

By combining (20) and (25) into (19), it is possible to obtain an approximation of the phase discriminator output $\delta\tilde{\theta}[n]$ by calculating

$$\delta\tilde{\theta}[n] = TZ^{-1}\left\{\left(1 - H(z)\right)\tilde{\theta}(z)\right\}[n]\,. \tag{26}$$

Analysis of the PLL structure during the tracking

Let us analyze a phase tracking with the PLL structure proposed in this section. Parameters of this tracking are the same as in the previous section so that Doppler dynamics used is fixed to 2Hz, the phase discriminator is chosen as an ATAN discriminator and all others parameters of the tracking loop are given in Fig. 9.

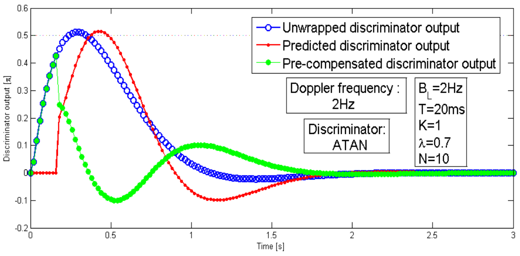

Fig. 9: Prediction and pre-compensation of discriminator output by analyzing loop filter output.

We can see in Fig. 9 the evolution of the prediction and pre-compensation step during the track. We can notice that predicted and pre-compensated discriminator outputs are not the same as illustrated in Fig. 4. This difference results from the transient time of the polynomial coefficients estimation which induces an error in the frequency to phase conversion stage (26). Once again we note in Fig. 10 that no cycle slip occurs although the phase discriminator outputs exceed the linear range of the discriminator. As expected, prediction of the discriminator output reduces the dynamics at the discriminator input. Since this reduced phase dynamics does not exceed the discriminator linear range, cycle slip is avoided.

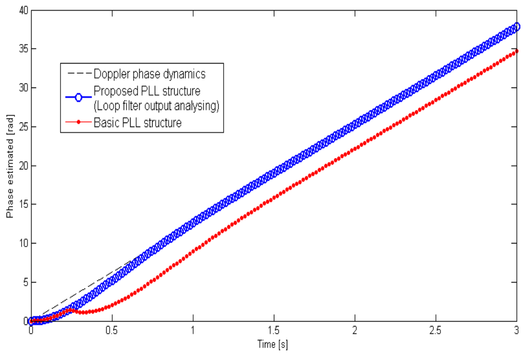

Fig. 10: Phase tracking for PLL basic structure and PLL structure analyzing loop filter output.

We can see in Fig. 11 the frequency polynomial coefficients estimates during the tracking.

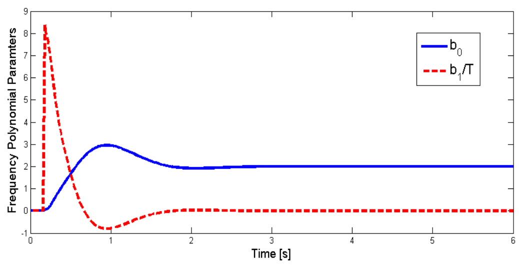

Fig. 11: Polynomial coefficients estimation for loop filter output analysis.

We notice that, when steady state is reached, these two coefficients correspond as expected to the frequency dynamics, i.e., $b_0=2$ and $b_1=0$ (frequency dynamics: 2Hz+0Hz/s).

RESULTS

In this section we study the noise robustness of the two PLL structures presented in this article. In order to highlight the robustness of these structures, we will compare them to a conventional PLL and another one that unwrap cycle slip by a thresholding method as described in [6]. To do so, a Doppler carrier phase dynamics will be fixed and tracked by all the four PLLs.
For the simulation that follows, the incoming signal will be generated as described in equation (1) and the Doppler carrier phase as

$$\phi[n] = \dot{\phi}(0) n T_e + \frac{1}{2}\ddot{\phi}(0) n^2 T_e^2 , \tag{27}$$

with $T_e=1/F_e$ (we work here on a L1 C/A signal with $F_e=2\times 1.023MHz$) and

$$\begin{aligned} \dot{\phi}(0)/2\pi &= 2Hz \\ \ddot{\phi}(0)/2\pi &= 0.5Hz/s \end{aligned} \tag{28}$$

which correspond to a pedestrian Doppler dynamics [17,18]. For the analysis model of the phase discriminator output and the loop filter outputs, the polynomial degree M will be fixed to 1, so outputs will be approximated by

$$\tilde{\theta}[n] = a_0 + a_1 n , \tag{29}$$

$$\tilde{\dot{\theta}}[n] = b_0 + b_1 n . \tag{30}$$

One can notice that, by fixing $M=1$ for the two proposed structures, we do not analyze the phase estimation error with the same degree. By estimating the parameters $\{b_0,b_1\}$ of equation (30), we can estimate the frequency dynamics and the phase acceleration; whereas the estimation of the parameters $\{a_0,a_1\}$ of equation (29) is just informing us about the phase and the frequency dynamics. This is one of the advantages of analyzing loop filter outputs: with the same degree of analysis, one can access to a higher phase dynamics. Unfortunately, by analyzing loop filter output, we lose the phase information. However, this loss of phase information is not so critical since a phase step dynamic does not imply steady state error contrary to higher dynamics.

The four discriminators used to compare PLLs are ATAN. The loop bandwidth is fixed at $B_L=3Hz$ (high enough to estimate the dynamics (28)) and the prediction time $T=20ms$ (because we assume here to work on a L1 C/A signal). For the two proposed PLLs, degree of the polynomial analysis is fixed to $M=1$ as said before. The

WRLS weight factor λ and the gain K are empirically determined and fixed to $\lambda=0.8$ and $K=0.6$. Concerning the thresholding PLL, a gain K is also present in the structure. This gain is fixed to $K=0.3$ as explained in [6].

is more robust to phase noise than the PLL structure analyzing discriminator output in term of loss of lock. This results from the fact that discriminator outputs are noisier than loop filter outputs and the analysis of the former then offers a better noise robustness.

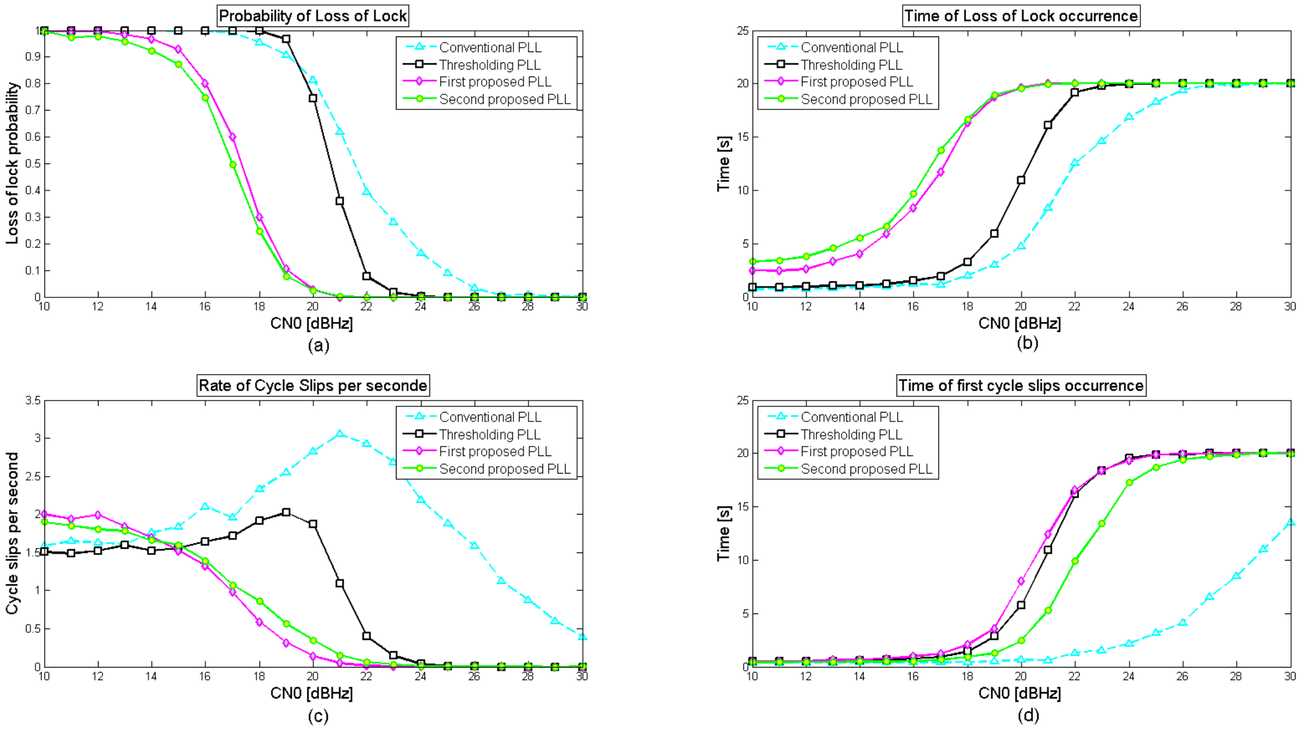

Fig. 12: Tracking performances of the two proposed PLL structures compared to the thresholding PLL and the conventional PLL.

Fig. 12 shows the average performance of the PLLs studied for 500 phase trackings of 20 seconds each. We can see, as a function of the CN0,

- The probability of loss of lock,
- The starting time of the loss of lock,
- The rate of cycle slips per second (based on the tracking time before losing the lock),
- The time of the first cycle slip.

When a cycle slip occurs, one can observe on phase estimation a transient time which corresponds to the time needed for the PLL to recover the steady state equilibrium. This transient time can be long enough to be considered as a local loss of lock. Thus, during the phase tracking, all transient times due to cycle slips that exceed *1s* (which corresponds roughly to the acquisition time of the loop [9]) are considered as a loss of lock.

We can see on Fig. 12 that, as expected, the two proposed methods have a better noise robustness than conventional and thresholding PLL structures. They decrease the loss of lock limit about 4~5 dBHz for this simulation as seen in Fig. 12(a). We can notice in Fig. 12(b) that the two proposed PLLs offer a longer time of phase tracking before losing lock. One can also see in Fig. 12(a) and Fig. 12(b) that the PLL structure analyzing loop filter outputs

Concerning cycle slips, we can see in Fig. 12(c) that the two proposed PLL structures have a better noise robustness in terms of cycle slips rate than the thresholding PLL structure. Indeed, for CN0 ranges that correspond to a reasonable probability of loss of lock of each PLL structures, we can see that the two proposed structures offer a lower cycle slips rate than the conventional and the thresholding PLLs. We can notice in Fig. 12(d) that the three unwrapping PLL structures have better performances than the conventional PLL in terms of time of the first cycle slip. This result can be obviously explained by the fact that the conventional PLL is the only one loop which does not possess an unwrapping system. Best performance is obtained with the first proposed PLL structure, followed by the threshoding structure and finally the second proposed structure. This last performance is quite conflicting with the fact that analysis of loop filter outputs is expected to be more robust and to offer a better cycle slips correction. However, this result can be explained by the presence of the additional conversion step (that converts loop filter prediction to discriminator prediction) which implies error of discriminator output prediction as explained before.

CONCLUSION

This paper has proposed two new unwrapping PLL structures that offer better noise robustness than conventional PLLs or PLLs using thresholding approach to correct cycle slips. These two structures are based on a system of prediction and pre-compensation of the forward discriminator output realized by analyzing the loop filter or discriminator output thanks to a polynomial analysis model.

Simulations show that, compared to threshold-based PLLs, the two proposed PLL structures have a better noise robustness in terms of loss of lock performance. Indeed, noise limits of loss of lock are decreased and time of phase tracking before the loss is increased.
Futures works will focus on adapting the proposed structures to multicarrier signals with the aim to enforce further the noise robustness of the loops and offer better performance in terms of cycle slips correction. The new generation of navigation signals (i.e., GALILEO signals) will also be used for testing the performances of the two proposed structures when they track a pilot signal with an ATAN2 phase discriminator.

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